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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/864,509	05/24/2001	Lee D. Whetsel	TI-31076	2438

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TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

EXAMINER	
BRITT, CYNTHIA H	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 12/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/864,509	WHETSEL ET AL.	
	Examiner	Art Unit	
	Cynthia Britt	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 2* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 2* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 May 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1 and 2 are presented for examination.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Cassetti et al. U.S. Patent No. 6,311,302.

As per claim 1, Cassetti et al. teach the claimed process of a circuit control arrangement for a multicore IC having a limited number of access pins for selecting functions internal to the IC. Where control is to be transferred between such TAP controllers of various core circuits such as: "In an example process for this control application, the extension bit has a special function and its use can be appreciated with reference to the arrangement 10 of FIG. 1 in the example process that follows. The process begins, for example, at reset time when the internal TLM for the core 12 is active and the TAP controller 16 within it is enabled. Sometime after reset, the internal TLM for the core 14 is to be enabled and the internal TLM for the core 12 disabled. For this scenario, the TAP controller 16 selects the TLM register 20 and shifts in a value that

sets the extension bit at 22. Since this extension bit is set, the TDI and TDO signals to the IC are now connected between the chip-level TLM 40 and the internal TLM for the core 12. In the next data loop, a command is shifted in the register internal to the chip-level TLM. At the end of the Update DR state for the TAP controller 16, the extension bit at 22 is cleared unconditionally. The new command thus shifted into the chip-level TLM 40 forces the TMS signal provided to the core 12 low, in turn forcing the TAP controllers 16 and 18 of the TLM'ed core 12 into IDLE state. At the same time, the TMS signal provided to the TLM'ed core 14 is enabled." (Abstract, Figures 1 and 2, column 2 line 60-67, column 5 line 58 through column 6 line 9)

Claim 2 is rejected under 35 U.S.C. 102(e) as being anticipated by Adusumilli et al. U.S. Patent No. 6,334,198.

As per claim 2, Adusumilli et al. teaches the claimed TAP linking module containing a TDI input and a TDO output, a TAP controller, registers for storing instructions and multiplexer having adequate support for the claimed connections (as also described in alternate embodiments of figure 1 - column 5 line 41-column 6 line 29). Adusumilli et al also teach a multiplexer connected with the TAP, TDI, TDO, as claimed. (Figure 1, abstract, column 4 lines 26-47, 53-65)

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

"*Hierarchical Test Access Architecture for Embedded Cores in an Integrated Circuit*" by Bhattacharya, D. VLSI Test Symposium Proceedings, Publication Date: 26-30 April 1998 pages 8-14 Inspec Accession Number: 6039765

This paper teaches that due to the rapid emergence of reusable core-based designs, new challenges to the IEEE test access standard 1149.1 arise. Due to widespread industrial acceptance of 1149.1 standard, ICs are now expected to be 1149.1-compliant. At the same time, a typical IC often contains multiple cores with built-in 1149.1 compliant Test Access Port (TAP), as well as significant amounts of non-core logic, which does not have any built-in test access mechanism. This paper presents a new TAP design that enables systematic integration of TAP'ed cores with non-TAP'ed logic, and makes the total IC 1149.1 compliant, at the same time. This TAP design, designated Hierarchical Test Access Port (HTAP), has exactly the same I/O pin specifications as an 1149.1-compliant TAP, and can either serve as an 1149.1-compliant TAP, or act as an arbitrator between existing TAPs in the Embedded cores. Behavior of the HTAP-whether to act as a TAP or as an arbitrator of TAPs-is controlled via the TMS input pin.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 571-272-3815. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Cynthia Britt
Examiner
Art Unit 2133